

Fig. 1

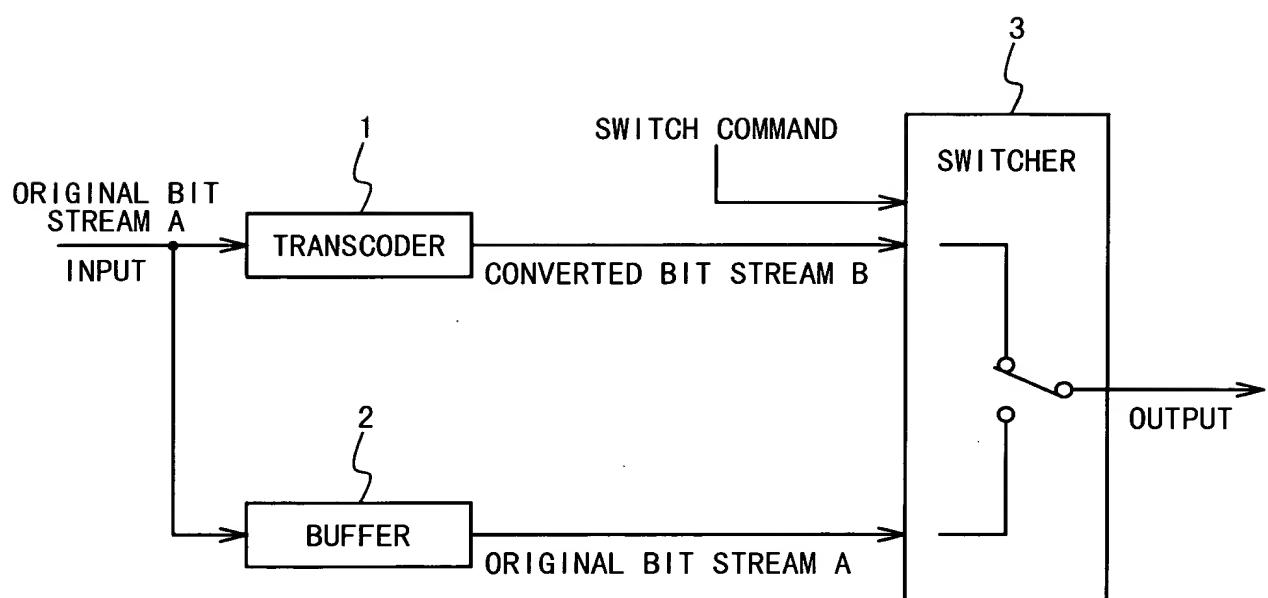


Fig. 2 A

INPUTTED ORIGINAL BIT STREAM A	A1	A2	A3	...

Fig. 2 B

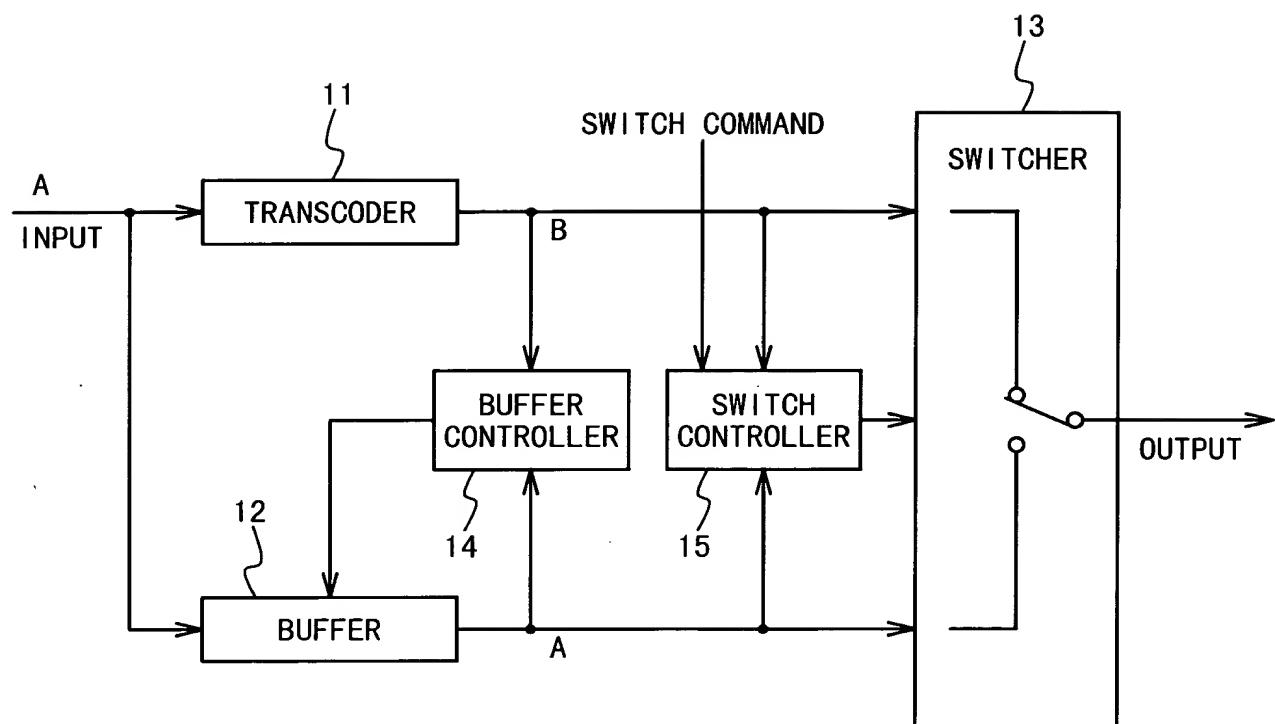
CONVERTED BIT STREAM B OUTPUTTED BY TRANSCODER 1	B1	B2	B3	...

Fig. 2 C

ORIGINAL BIT STREAM A OUTPUTTED BY BUFFER 2	A1	A2	A3	...

050222Z APR 60

Fig. 3



APPROVED	O. F. FIG.
BY	C. S. S. H. S.
DRAFTMAN	

Fig. 4 A

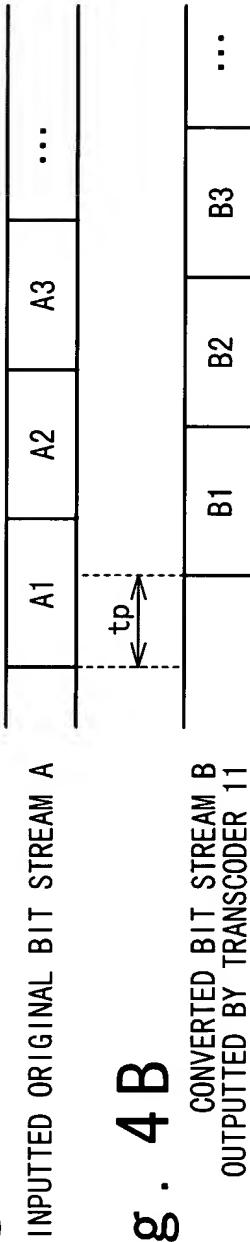


Fig. 4 B

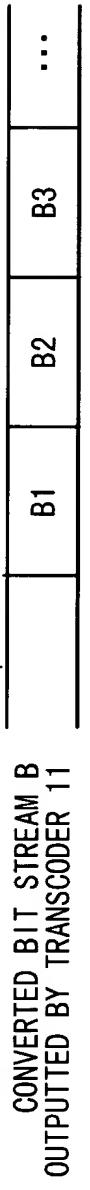


Fig. 4 C

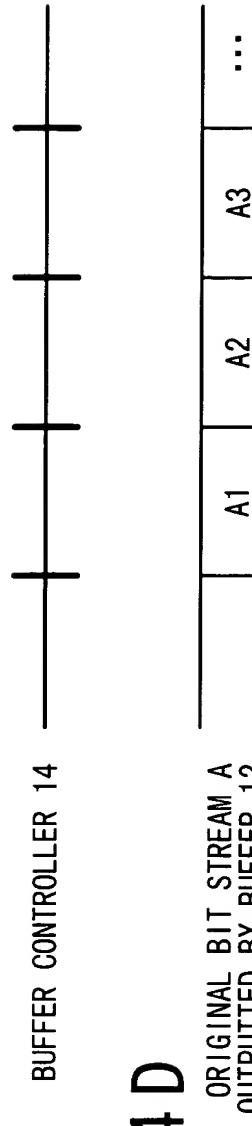


Fig. 4 D

APPROVED	10/2/11 G.
BY	Chas. S. H.
CHIEF	
CHIEF	

卷之三

F i g . 5 A	ORIGINAL OR CONVERTED BIT STREAM
F i g . 5 B	SWITCH COMMAND
F i g . 5 C	SWITCH CONTROLLER 15

